REMARKS

Reconsideration and allowance of this application, as amended, is respectfully requested.

This amendment is in response to the Office Action dated December 7, 2006. By the present amendment, the original claims 1-9 have been cancelled, without prejudice, and replaced with new independent claim 10 and its dependent claims 11-14. These new claims have been drafted to remove the phraseology noted in the 35 U.S.C. §112, second paragraph, rejection and the claim objections set forth on page 2 of the Office Action. Therefore, reconsideration and removal of the 35 U.S.C. §112, second paragraph, rejection and the claim objections is respectfully requested.

Briefly, the present invention is directed to an improved semiconductor device which incorporates an ECC together with a parallel test mode to provide improved accuracy with a simplified structure and shortened test times (e.g. see paragraph [0008]of the published United States Application 2004/0184327 for this application.) Referring, solely for purposes of example, to Figure 1, an embodiment utilizing a D-RAM chip 100 includes an ECC decoder 108 and parallel test decision circuits 109. As described in paragraph [0047] of the published application:

> In the DRAM according to the present invention, as described later, one of the objects to employ the ECC is to cope with retention defect of memory data. In other words, the refresh interval (cycle) of the DRAM is made longer. In this case, when there is a 1-bit defect in 8+4 bits as an ECC unit, it must be decided as a non-defective product. As described above, however, in the parallel test for deciding whether all bits are in coincidence or not, the 1-bit defect is decided as being rejected. To avoid this, a method for testing all bits without using the parallel test can be considered. It increases the test cost, which is hard to accept.

Accordingly, paragraph [0048] describes a feature of the present invention which is utilized to avoid this undesirable increase in test cost, specifically:

> Accordingly, the present invention employs a parallel decision circuit corresponding to the ECC. Since any retention deflect by the ECC, an acceptance decision is given to a 1-bit defect in 8+4 bits. There requires a parallel decision circuit for detecting 1-bit non-coincidence as well as all bits coincidence to output an acceptance decision.

In addition, another feature of the present invention is described in paragraph [0053] which states:

> "when there is 1-bit non-coincidence in all bits, there is 2-bit non-coincidence in all bits and the respective non-coincidence bits exist in another ECC relief unit, Hi is outputted. In another bit pattern Lo is outputted."

Therefore, the end result is an arrangement in which an ECC unit and a parallel test mode can operate to provide more accurate results without undesirable increases in test time and cost.

Reconsideration and allowance of newly presented independent claim 10 over the primary reference of USP 6,295,617 to Sonobe, whether considered alone or in combination with the secondary cited references, including USP 5,430,742 to Jeddelow is respectfully requested. By the present amendment, a combination of features is defined in the independent claim 10 which includes an error correcting circuit in conjunction with the semiconductor memory device being adapted to include a parallel test mode. Specifically, the present claims define, in addition to the error correcting circuit, parallel test circuits that are adapted to be activated during the parallel

test mode and which are coupled to the error corrected circuit. In particular, independent claim 1 defines:

> "the parallel test circuits are adapted to detect a 1-bit information code defect by the correction unit during the parallel test mode."

This corresponds, for example, to the above-noted discussion from paragraph [0048] of the published application.

It is respectfully submitted that the Sonobe reference completely fails to teach or suggest this claimed combination of an ECC circuit and parallel decision circuits which perform a parallel test mode to detect a 1-bit information code defect by the correction unit during the parallel test mode. On the contrary, Sonobe is of general interest with regard to teaching an ECC circuit, but completely fails to teach or suggest the features defined by independent claim 10, of parallel test circuits which are activated during the parallel test mode and which are coupled between the ECC circuit and each of the plurality of memory amounts, as defined by independent claim 10. Therefore, reconsideration and allowance of newly submitted independent claim 10 over Sonobe, whether considered alone or in combination with the other cited prior art in this case is respectfully requested.

Reconsideration and allowance of the newly dependent claims 11-14 is also respectfully requested. In each case, these define further features of the present invention, corresponding to features discussed, for example, in paragraphs [0048] and [0053] which are completely unsuggested by the Sonobe reference, whether considered alone or in combination with the other cited prior art. For example, dependent claim 11 specifically defines that the parallel test circuits are adapted to decide not only that the one bit information

code defect is an acceptance decision, but also that an all bit information code coincidence is an acceptance decision. This corresponds to the above-noted statement in paragraph [0048] that both 1-bit defects and all bits coincidence are acceptance decisions, contrary to the situation described in paragraph [0047] which would cause an undesirable increase in test cost. Dependent claim 12 defines the situation described, for example, in paragraph [0053] in which the parallel test circuit are adapted to decide not only that a 1-bit information code defect is an acceptance decision, but also that a 2-bit information code defect which exists in a different correction unit is an acceptance decision. Therefore, it is urged that these dependent claims 11-14 even further define over the Sonobe reference, whether considered alone or in combination with the other cited prior art. Therefore, reconsideration and allowance of newly presented claims 12-14 is earnestly solicited.

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of either by telephone discussion or by personal interview, the Examiner is invited to contact Applicants' undersigned attorney at the number indicated below.

To the extent necessary, Applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to

Deposit Account No. 01-2135 (Case No. 501.43354X00) and please credit any excess fees to such deposit account.

Respectfully submitted,

Gregory E. Montone
Registration No. 28,141
ANTONELLI, TERRY, STOUT & KRAUS, LLP

GEM/kmh

Attachments